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Abstract of the Disclosure

An EEPROM having a memory cell array in which electrically programmable memory cells are arranged in a matrix and each of the memory cells has three storage states, includes a plurality of data circuits for temporarily storing data for controlling write operation states of the plurality of memory cells, a write circuit for performing a write operation in accordance with the contents of the data circuits respectively corresponding to the memory cells, a write verify circuit for confirming states of the memory cells set upon the write operation, and a data updating circuit for updating the contents of the data circuits such that a rewrite operation is performed to only a memory cell, in which data is not sufficiently written, on the basis of the contents of the data circuits and the states of the memory cells set upon the write operation. A write operation, a write verify operation, and a data circuit content updating operation based on the contents of the data circuits are repeatedly performed until the memory cells are set in predetermined written states.